COMMON CENTROID LAYOUT FOR PARALLEL RESISTORS IN AN AMPLIFIER WITH MATCHED AC PERFORMANCE

ABSTRACT OF THE DISCLOSURE

Common centroid layout for parallel resistors in an amplifier with matched AC performance. An amplifier is disclosed that is formed on a silicon substrate that includes first and second differential legs, each driving first and second resistive loads. The first resistive load comprises first and second parallel resistive loads connected on one side thereof to one end of the first differential leg and the other side of each of the first and second parallel resistive loads separately connected to a first reference voltage. The second resistive load comprises third and fourth resistive loads each connected on one side thereof to one end of the second differential leg and the other side of each of the third and fourth parallel resistive loads connected separately to the first reference voltage. Each of the first, second, third and fourth resistive loads is fabricated of a strip of resistive material disposed on the surface of the substrate and having a finite resistivity, length, width and thickness. The first parallel resistive load is disposed adjacent to a first dummy resistive strip on one side thereof, and disposed adjacent the third parallel resistive load on the opposite side thereof. The third parallel resistive load is disposed adjacent a second dummy resistive strip disposed on the diametrically opposite side thereof from the first parallel resistive load. The fourth parallel resistive load is disposed adjacent the second dummy resistive strip on the diametrically opposite side thereof from the third parallel resistive load. The second resistive load is disposed adjacent the fourth parallel resistive load and capacitively coupled thereto on the side diametrically opposite to the second dummy resistive strip. The second parallel resistive load is disposed adjacent a third dummy resistive strip on the side thereof diametrically opposite to the fourth parallel resistive load and capacitively coupled thereto. The first, second and third dummy resistive strips are connected to a second reference voltage.